Set No. 1

IV B.Tech II Semester Regular Examinations, Apr/May 2007
EMBEDDED SYSTEMS
(Common to Electrical & Electronic Engineering and Electronics &
Communication Engineering)

Time: 3 hours   **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. What is NRE cost? For a particular product determine the NRE cost and unit cost to be for the following three listed IC technologies:
   FDGA: ($10,000,$50)
   ASIC: ($50,000,$10)
   VLSI: ($200,000,$5). [16]

2. Design a 2-bit comparator with a single output, using the combination logic design architecture. [16]

3. Describe why a general-purpose processor would cost less than a single-purpose processor you design yourself. [16]

4. State the need for more functional units in digital signal processor. [16]

5. Explain in detail about Hierarchical/Concurrent state machine models. [16]

6. Explain the concept of synchronization among concurrent processes by condition variables with an example. [8+8]

7. Design a circuit for the expression F=abc'd'+a'cd+ab'cd with minimum gates using two level logic minimization. [16]

8. Explain in detail about intellectual property cores. [16]

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Set No. 2

IV B.Tech II Semester Regular Examinations, Apr/May 2007
EMBEDDED SYSTEMS
(Common to Electrical & Electronic Engineering and Electronics & Communication Engineering)

Time: 3 hours
Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks
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1. List a pair of design metrics that may compete with one another, providing an intuitive explanation of the reason behind the competition. [16]

2. (a) What is a single-purpose processor? What are the benefits of choosing a single-purpose processor to against a general-purpose processor?
   (b) Draw the basic architecture of single-purpose processor. [8+8]

3. (a) Explain the factors effecting selection of a microprocessor.
   (b) Compare the general purpose processor, microcontroller and Digital signal processor. [8+8]

4. Explain the need of special architecture for pipelining and parallelism. [16]

5. (a) What are the models commonly used for describing embedded systems?
   (b) State differences between a computation model and a language, and also between a textual language and a graphical language. [8+8]

6. (a) Describe the concurrent process model with an example.
   (b) Distinguish between computational models, languages and implementations. [8+8]

7. Describe each tool that has enabled the elevation of software design and hardware design to higher abstraction levels. [16]

8. (a) What is hardware /software co-design?
   (b) Explain temporal and spatial thinking in hardware/software co-design? [8+8]

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Set No. 3

IV B.Tech II Semester Regular Examinations, Apr/May 2007
EMBEDDED SYSTEMS
(Common to Electrical & Electronic Engineering and Electronics &
Communication Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is an embedded system? Why is it so hard to define?
   (b) List the applications of embedded systems. [8+8]

2. Design a 3-bit counter that counts the following sequence: 1,2,4,5,7,1,2,?.. start from a state diagram, draw the state table, minimize the logic, and draw the final circuit. [16]

3. (a) Explain the general purpose processor design.
   (b) Draw and explain architecture of a simple microprocessor. [8+8]

4. Explain different data addressing modes of digital signal processor. [16]

5. Explain in detail about Hierarchical/Concurrent state machine models. [16]

6. (a) Describe the concurrent process model with heart beat monitoring embedded system.
   (b) Illustrate the Set top box embedded system. [8+8]

7. Describe each tool that has enabled the elevation of software design and hardware design to higher abstraction levels. [16]

8. (a) Explain the three types of cores such as hard, soft and firm cores.
   (b) Show the correspondence of the three types of cores with Gazki's Y-chart. [8+8]

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Set No. 4

IV B.Tech II Semester Regular Examinations, Apr/May 2007
EMBEDDED SYSTEMS
(Common to Electrical & Electronic Engineering and Electronics &
Communication Engineering)

Time: 3 hours **Max Marks: 80**
Answer any FIVE Questions
All Questions carry equal marks
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1. List and define the three main processor technologies. What are the benefits of using each of the three different processor technologies? [16]

2. Design a 3-bit counter that counts the following sequence: 1,2,4,5,7,1,2,.. start from a state diagram, draw the state table, minimize the logic, and draw the final circuit. [16]

3. Explain the following in embedded systems view:

   (a) Program and Data memory space.

   (b) Registers.

   (c) I/O.

   (d) Interrupts. [4+4+4+4]

4. Explain the need of special architecture for pipelining and parallelism. [16]

5. Explain the state chart language with elevator controller example. [16]

6. (a) Explain different processes scheduler in a single general purpose processor.

   (b) Explain different types of scheduling algorithms in a single processor environment. [8+8]

7. List and describe three general approaches to improving designer productivity.[16]

8. Explain in detail about intellectual property cores. [16]

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